

# INVENTOR INFORMATION

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## CORRESPONDENCE INFORMATION

Correspondence Customer Number:: 000023548  
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## APPLICATION INFORMATION

Title Line One:: SEMICONDUCTOR INTEGRATED CIRCUIT COMPRIS  
Title Line Two:: ING SYNCHRONOUS DRAM CORE AND LOGIC CIRC  
Title Line Three:: UIT INTEGRATED INTO A SINGLE CHIP AND ME  
Title Line Four:: THOD OF TESTING THE SYNCHRONOUS DRAM COR  
Title Line Five:: E  
Total Drawing Sheets:: 15  
Formal Drawings?: Yes  
Application Type:: Utility Reissue  
Docket Number:: 401191  
Secrecy Order in Parent Appl.?: No

#### REPRESENTATIVE INFORMATION

Representative Customer Number:: 23548

#### CONTINUITY INFORMATION

This application is a:: REISSUE OF  
> Application One:: 08/964,236  
Filing Date:: 11-04-1997  
Patent Number:: 5,910,181

#### PRIOR FOREIGN APPLICATIONS

Foreign Application One:: 9-086600  
Filing Date:: 04-04-1997  
Country:: Japan  
Priority Claimed:: Yes

Source:: PrintEFS Version 1.0.1

08/964,236